Double side interconnection for vertical power components based on macro and nano structured copper interfaces and printed circuit board technologies

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OUTLINE

Introduction

Context

Manufacturing process

Experimental results

Conclusion

INTRODUCTION

Stronger power ratings ensured by

1. Interleaved topologies : Multicellular structures
   - Reducing of passive components size
   - Active components multiplying
2. Switches improvement : Wide band gap materials
   - Increasing of switching frequency
   - Higher working temperature

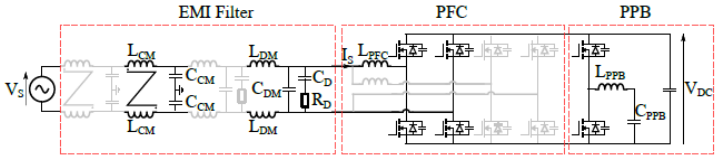

Figure 1: 3.3 kW ac/dc converter with SiC power devices

Active switches integration is sought

1. Reduce stray elements (and size)
2. Enhancement of thermal management (reliability)

INTRODUCTION

Motivation

Electrical challenges

1. **Parasitic inductances**
   - Overvoltage due to high di/dt (L_{PC} & L_{PE})
   - Slow down switching time (L_{PG} & L_{PE})
2. **Parasitic capacitances**
   - Ringing with parasitic inductances (C_{PCE})
   - Common mode current ($C_{P\ OUT}$)
3. **Parasitic resistances**
   - Voltage drop

Heat dissipation from

1. **Switches losses**
2. **Interconnections losses** *(especially wire-bonds)*

Reliability

1. **Different CTE** combined with thermal cycling
2. **Capable of handling many thermal cycling** before failure

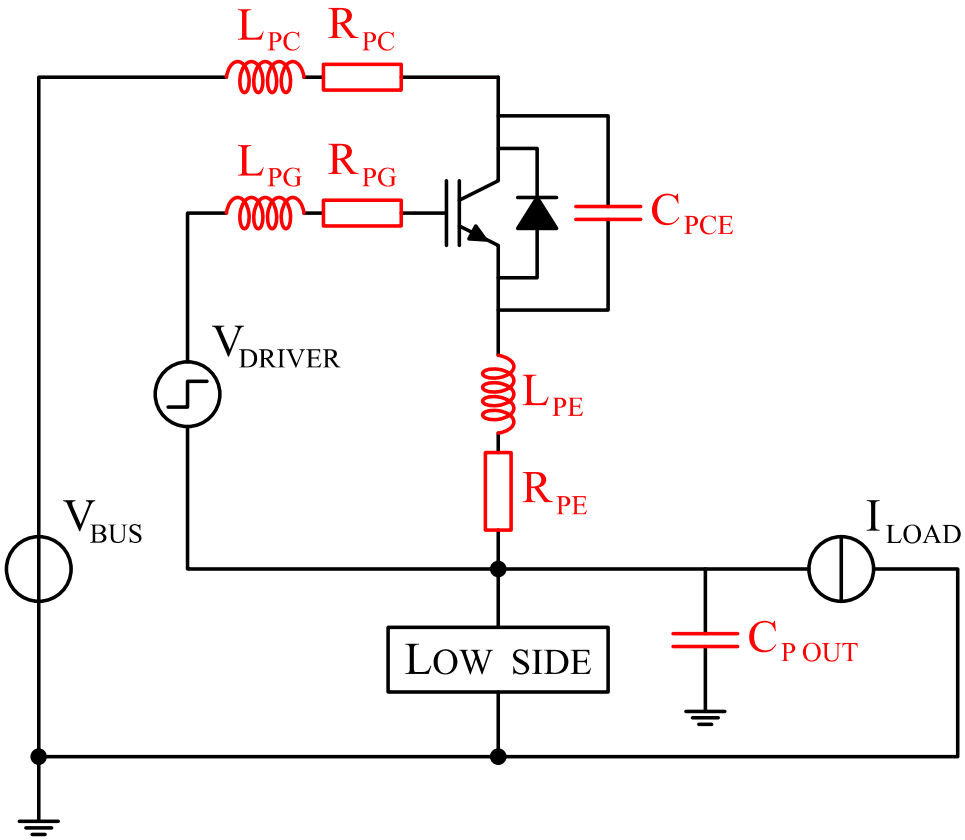

Figure 2: Zoom on parasitic elements (red) of the high side switching cell induced by the packaging

OUTLINE

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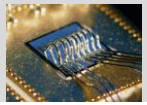
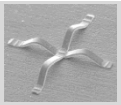
CONTEXT

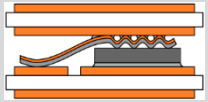
Interconnection state-of-the-art

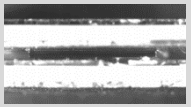
Bonding

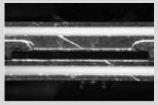

Wire bonding


Ribbon bonding

Soldering

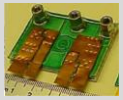

Bimetallic ribbon


Direct solder

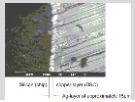

Metal post

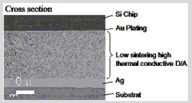

Solder bump


Direct lead bonding


Dimple array

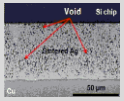
Sintering


Low Temperature Joining Technology



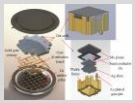
Low Temperature and Pressureless Sintering Tech.

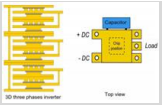
Diffusion bonding

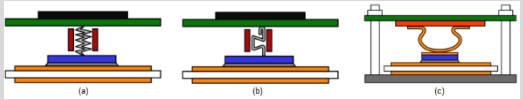


Transient Liquid Phase Bonding

Pressed

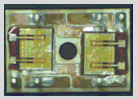

Press pack


Low force 3D



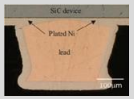
Springs

Electroplating


Power Overlay

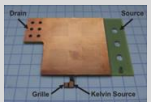

Embedded Power


SiPLIT

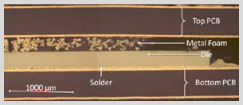


Nickel Micro Plating Bonding

PCB technologies



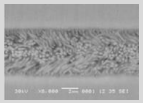
Micro vias



Foams

Structured interface


Micrometric scale (post)


Nanometric scale (tube and wire)

CONTEXT

Printed Circuit Board (PCB)

Printed Circuit Board (PCB) technology is

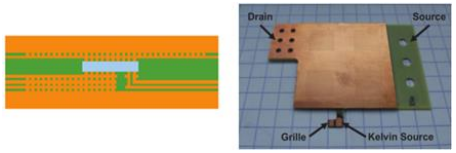
- Cost efficient and well-established process
- Offering massive parallel manufacturing
- Capable of fine pitch and able to use thick copper (heat and current transport)
- Accurate repeatable multilayer structures
- Fan-out capable
- Minimizing of loop size (stray inductances)

PCB-embedding offers

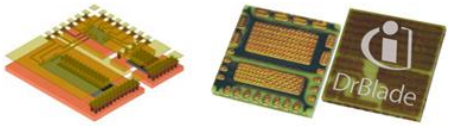
1. Double sided thermal dissipation and shorter heat path
2. Short interconnections and low parasitics
3. Increasing power density (by size reducing)

Laser micro vias

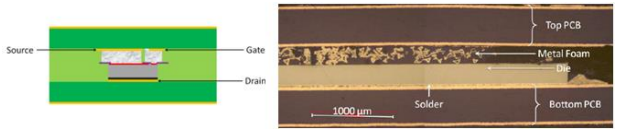
- Is the trend in PCB embedding interconnection
- Suffer of heat flux limitations (manufacturing limits)



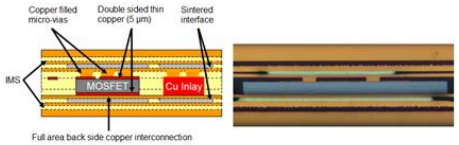
Full µVias interconnections



diffusion bonding and µVias interconnections



Soldering and foam interconnections



Galvanic Cu and vias interconnections

µVias and sintering interconnections

CONTEXT

Assembly

Proposed solution combines

- PCB substrates **(a)**
- having a macro post and nano wires interconnection
- sandwiching a die **(d)** surrounded of core **(c)**
- assembled by thermo-compression of prepregs **(b)**

High level of integration

1. Double-side cooling possible (symmetrical structure)
2. Full copper and flexible interconnection
3. Expected resistant to cyclical stresses
4. Elementary block for power converter

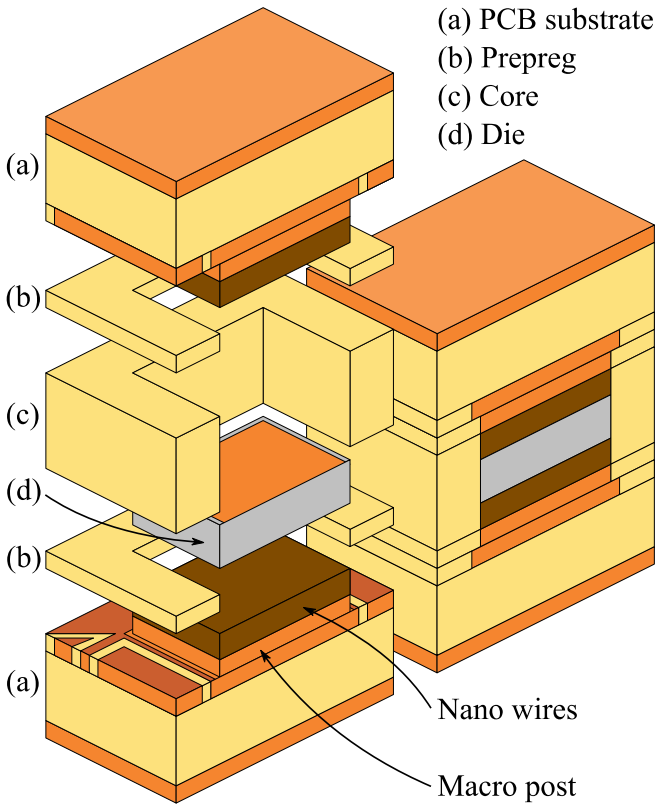


Figure 3: Cross section schematic of the assembly with macro and nano structured interfaces

SUMMARY

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Manufacturing process

Experimental results

Conclusion

MANUFACTURING PROCESS

PCB substrate functions

A 0.8 mm high temperature core with two 105 µm thick copper layers

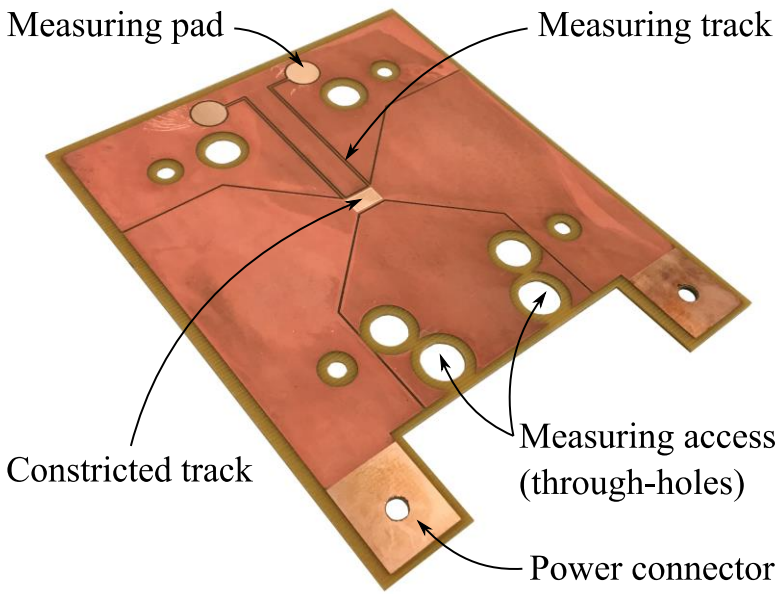


Figure 4: PCB substrate with constricted area, its connectors and kelvin measuring tracks

Power connectors

- For electrical and thermal characterization

Constricted area

- Bare copper area for the interconnection manufacturing
- Constriction is done for helping thermal characterization

Measuring pads and **tracks**

- Additional contacts for Kelvin measurements

Measuring accesses

- To the opposite substrate measuring pads

Brown oxidized remainder copper and ground planes to increase prepreg adhesion

MANUFACTURING PROCESS

Interconnection

- **Opened dry film on constricted area**

a. Dry film deposition (≈ 45 µm) on the whole PCB surface;
b. Opening of the dry film over the constricted area.

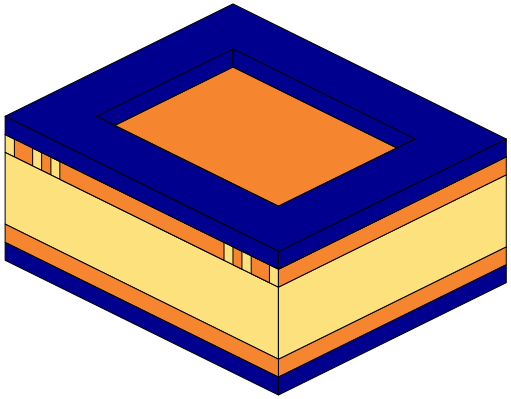


Figure 5: Manufacturing process of interconnection on the PCB substrate

MANUFACTURING PROCESS

Interconnection

Opened dry film on constricted area

- **Copper electro-etching on the constriction**

a. ≈ 7 µm copper electro-etching (pulsed waveform) to increase adhesion of the surface.

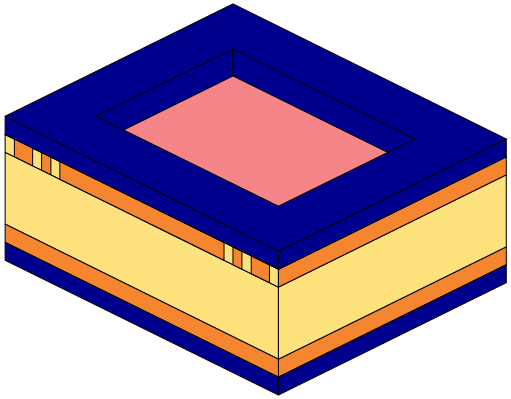


Figure 5: Manufacturing process of interconnection on the PCB substrate

MANUFACTURING PROCESS

Interconnection

Opened dry film on constricted area
Copper electro-etching on the constriction

- **Macro post electroplating (overflowing of dry film)**

a. ≈ 60 µm copper electroplating (pulsed waveform) The electroplating profile is adjusted to have the top of the post slightly higher than the dry film to ensure a complete filling of the cavity.

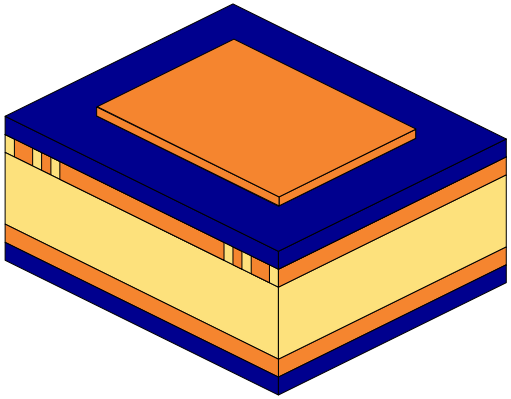


Figure 5: Manufacturing process of interconnection on the PCB substrate

MANUFACTURING PROCESS

Interconnection

Opened dry film on constricted area
Copper electro-etching on the constriction
Macro post electroplating (overflowing of dry film)

- **Leveling of the macro post by electro-etching**

a. ≈ 7 µm copper electro-etching (pulsed waveform) The copper post is etched to obtain a flushed surface between the dry film and the copper post. This is the condition to ensure a correct sealing for the forthcoming steps.

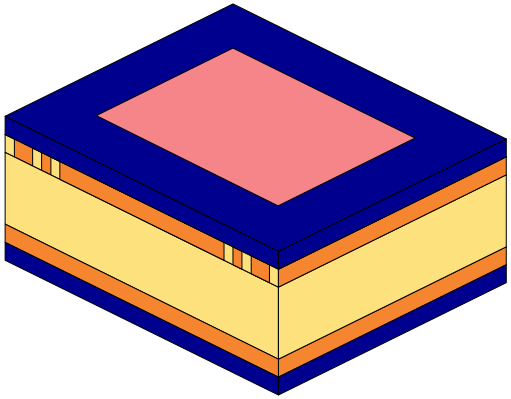


Figure 5: Manufacturing process of interconnection on the PCB substrate

MANUFACTURING PROCESS

Interconnection

Opened dry film on constricted area
Copper electro-etching on the constriction
Macro post electroplating (overflowing of dry film)
Leveling of the macro post by electro-etching

- **Nano wires electroplating by pressed anode**

a. A nanoporous membrane is placed on top of the copper post;
b. A solution of copper sulfate is spread over to act as an initiator;
c. 2 layers of cellulosic papers are added on top as solution buffer;
d. A copper anode is pressed on top of this assembly;
e. Copper is electroplated during ≈ 1 hour through the membrane using a pulsed waveform.

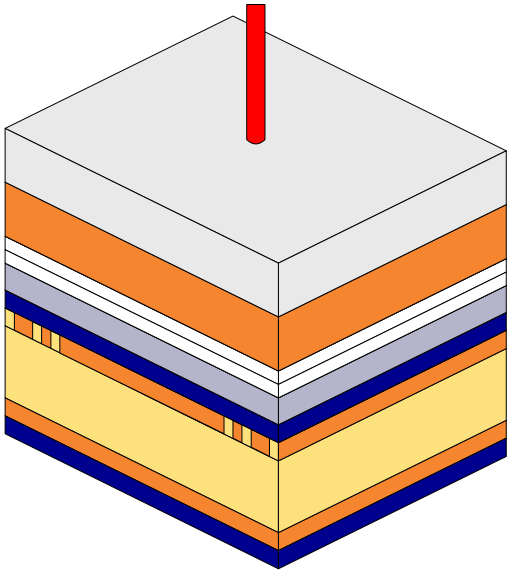


Figure 5: Manufacturing process of interconnection on the PCB substrate

MANUFACTURING PROCESS

Interconnection

Opened dry film on constricted area
Copper electro-etching on the constriction
Macro post electroplating (overflowing of dry film)
Leveling of the macro post by electro-etching
Nano wires electroplating by pressed anode

- **Membrane filling by distanced anode**

Once the electrodeposition have been initiated

a. The 2 layers of cellulosic papers are removed;
b. The anode is placed further away;
c. ≈ 6 hours copper electroplating is done until the membrane is filled.

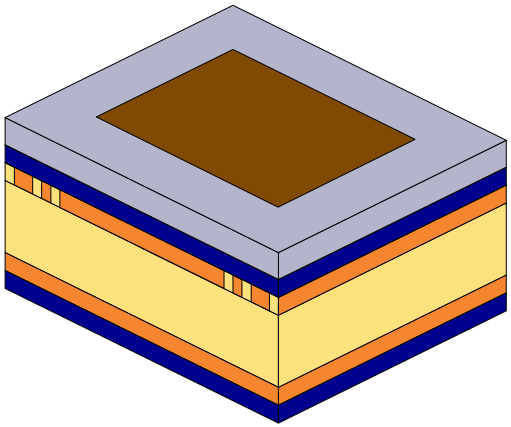


Figure 5: Manufacturing process of interconnection on the PCB substrate

MANUFACTURING PROCESS

Interconnection

Opened dry film on constricted area
Copper electro-etching on the constriction
Macro post electroplating (overflowing of dry film)
Leveling of the macro post by electro-etching
Nano wires electroplating by pressed anode
Membrane filling by distanced anode

- **Dry film and membrane removal**

a. Sodium hydroxide treatment at 45°C during half an hour.

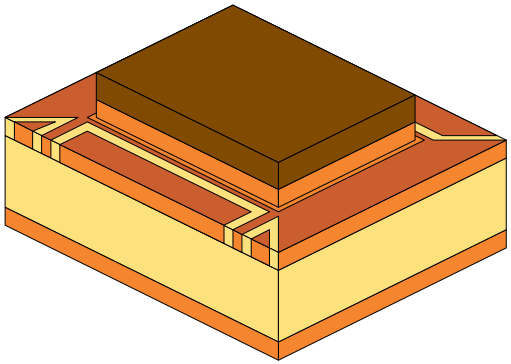


Figure 5: Manufacturing process of interconnection on the PCB substrate

MANUFACTURING PROCESS

Interconnection

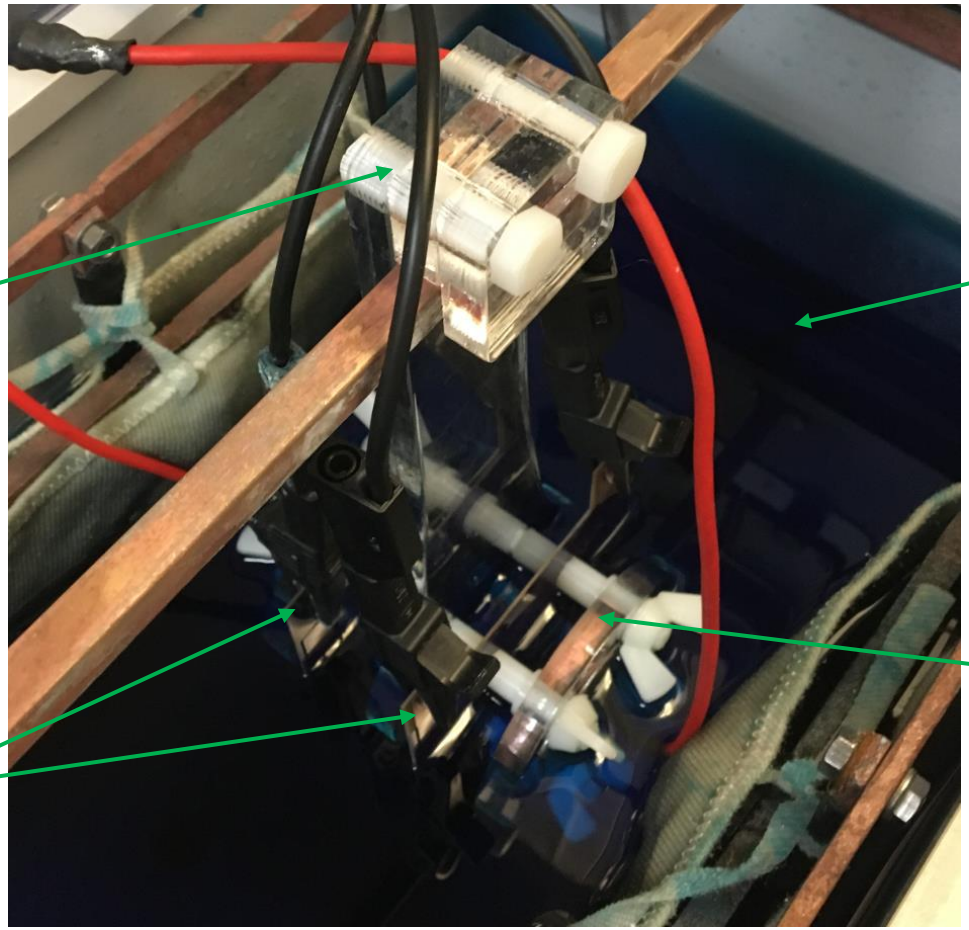


Figure 6: Nano wires electroplating on 2 parallel substrates with Bungard COMPACT A equipment

MANUFACTURING PROCESS

Interconnection

Full copper interconnection : 45 µm macro post and 55 µm nano wires of 200 nm diameter

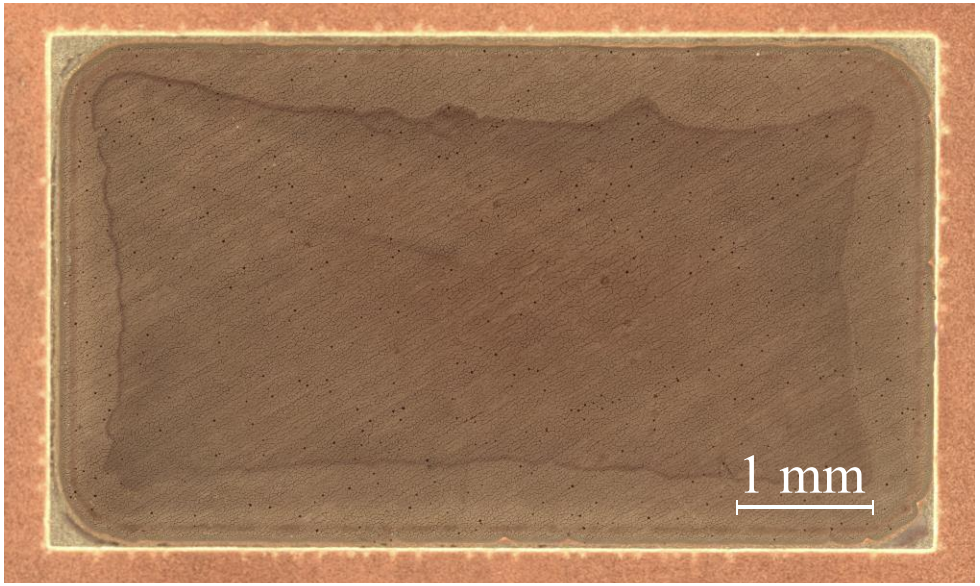


Figure 7: Digital microscope picture (x200) of the macro and nano structured interface

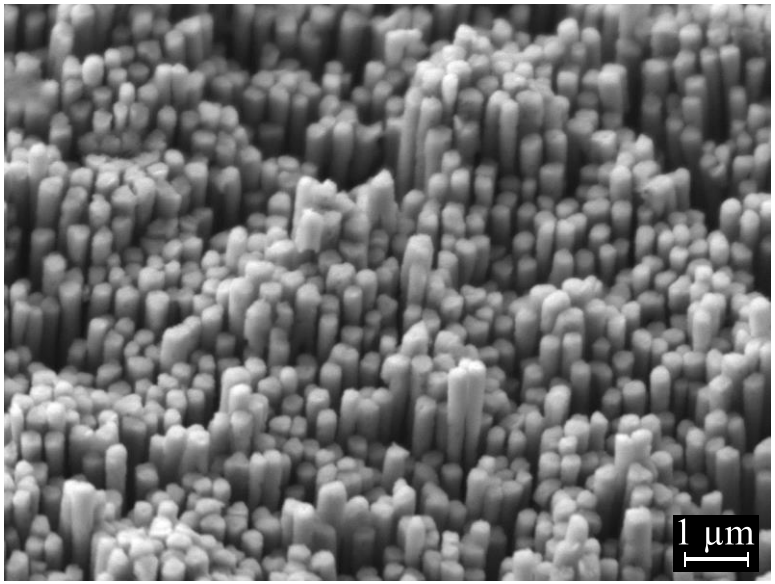


Figure 8: SEM acquisition (x10,000) of the nano wires 40° tilted top view

- Consistent and continuous = good heat and current transport
- Nano wires well separated = flexible stress resistant interface

MANUFACTURING PROCESS

Test vehicles assembly

- **Preparation of the support**

a. Bottom plate;
b. 4 centering pins;
c. 1st release film;
d. Conformable press pad;
e. 2nd release film.

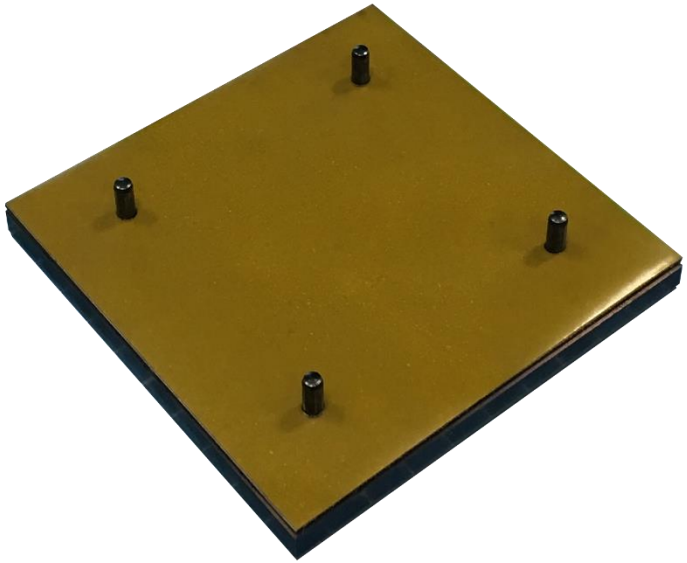


Figure 9: Stacking of the different elements of the prototype

MANUFACTURING PROCESS

Test vehicles assembly

Preparation of the support

- **Macro-nano structured PCB substrate**

a. Deoxidized by 10% sulfuric acid treatment;
b. 12 hours annealing at 120°C.

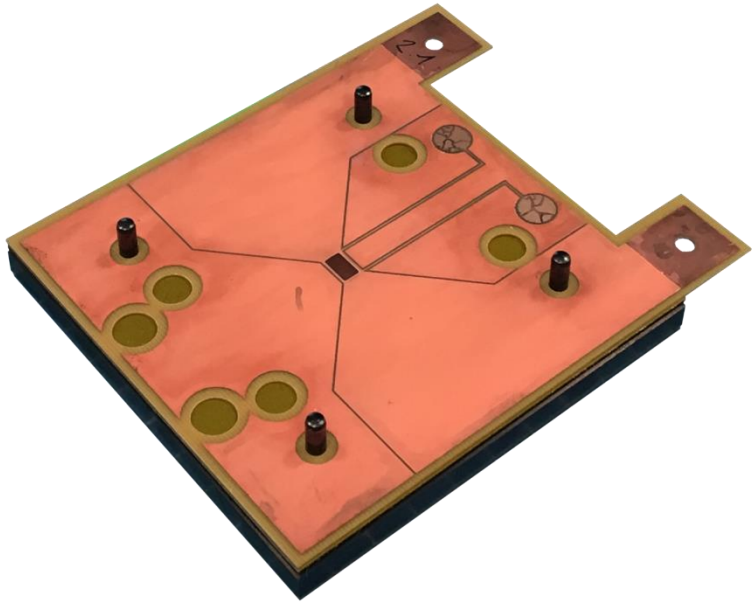


Figure 9: Stacking of the different elements of the prototype

MANUFACTURING PROCESS

Test vehicles assembly

Preparation of the support
Macro-nano structured PCB substrate

- **Prepreg Arlon 35N 106**

a. Laser cut-out.

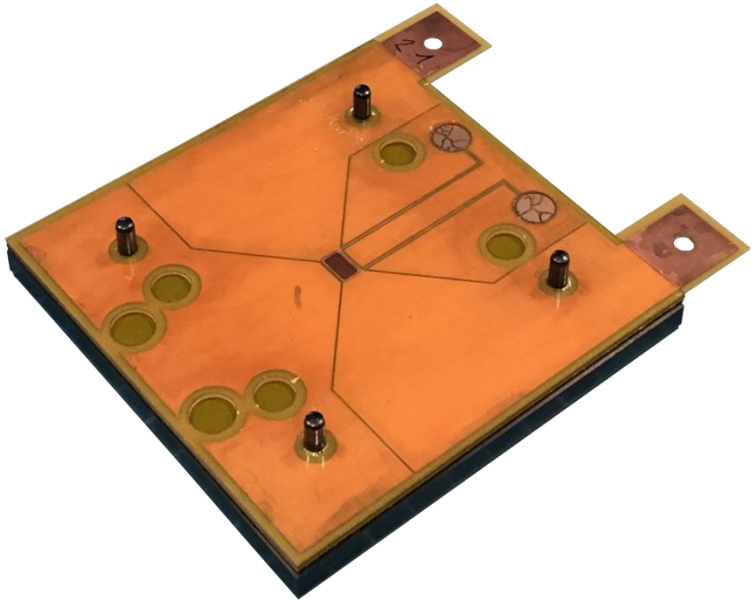


Figure 9: Stacking of the different elements of the prototype

MANUFACTURING PROCESS

Test vehicles assembly

Preparation of the support
Macro-nano structured PCB substrate
Prepreg Arlon 35N 106

- **Core Arlon 35N**

a. Stratification of prepregs Arlon 35N (1 × 2116, 1 × 1080 and 2 × 106);
b. Through holes and routing by CNC device.

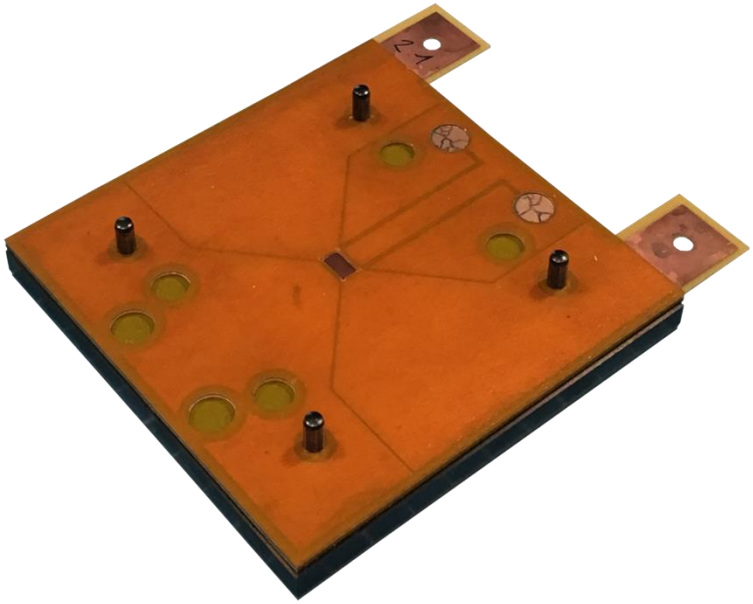


Figure 9: Stacking of the different elements of the prototype

MANUFACTURING PROCESS

Test vehicles assembly

Preparation of the support
Macro-nano structured PCB substrate
Prepreg Arlon 35N 106

- **Core Arlon 35N**

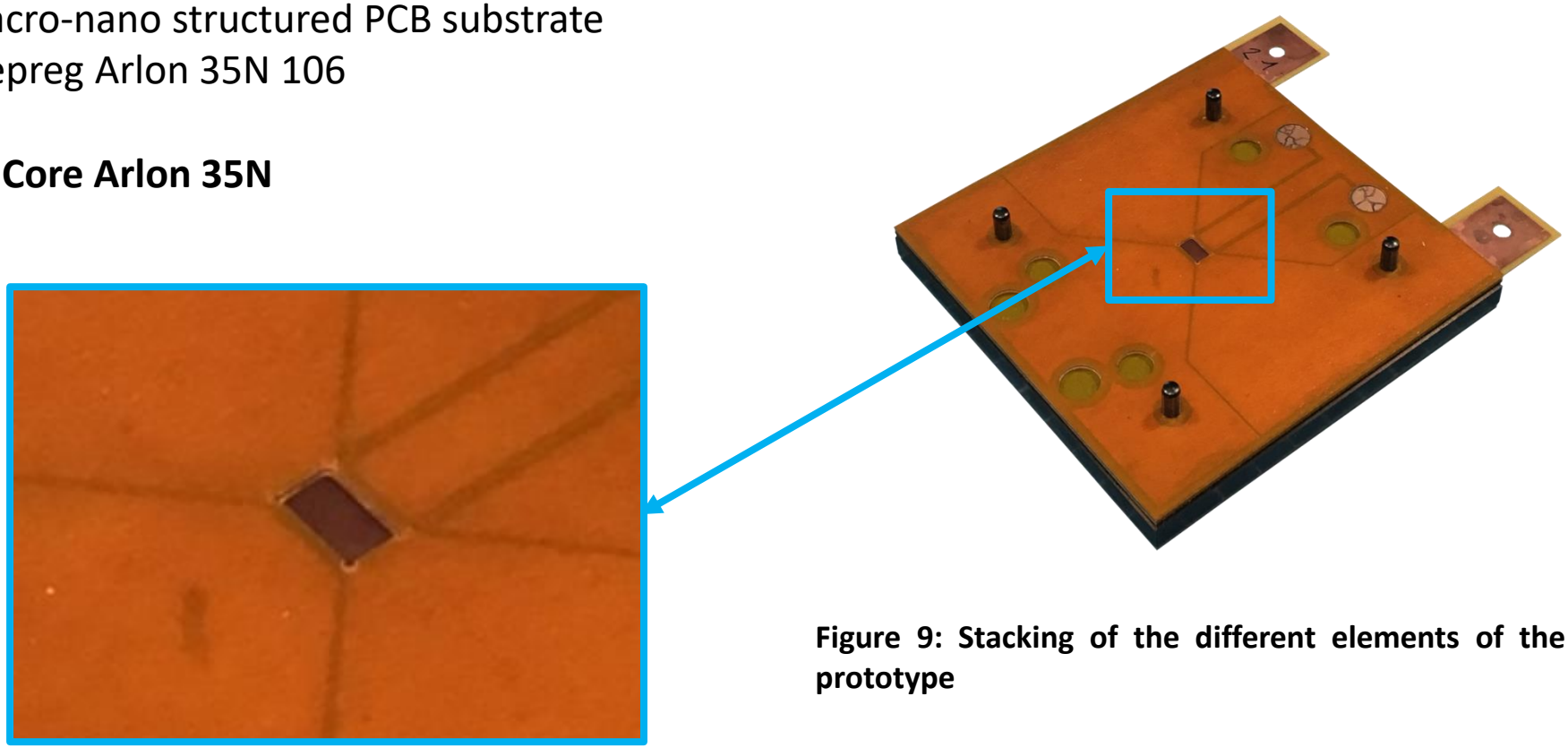


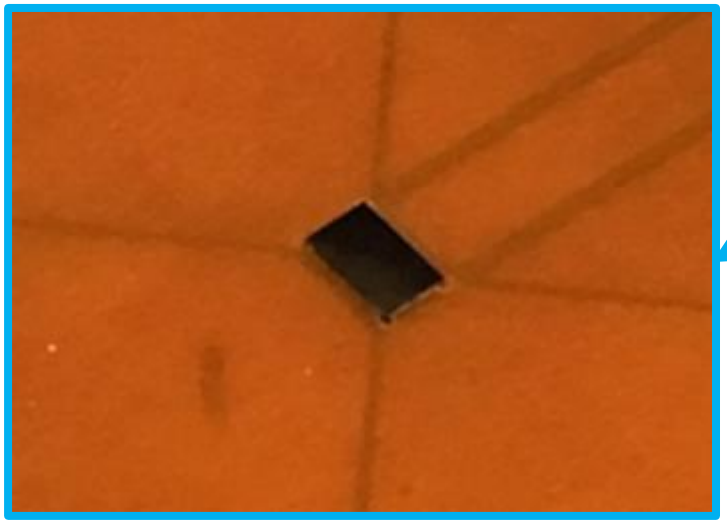
Figure 9: Stacking of the different elements of the prototype

MANUFACTURING PROCESS

Test vehicles assembly

Preparation of the support
Macro-nano structured PCB substrate
Prepreg Arlon 35N 106
Core Arlon 35N

- **Bare die**



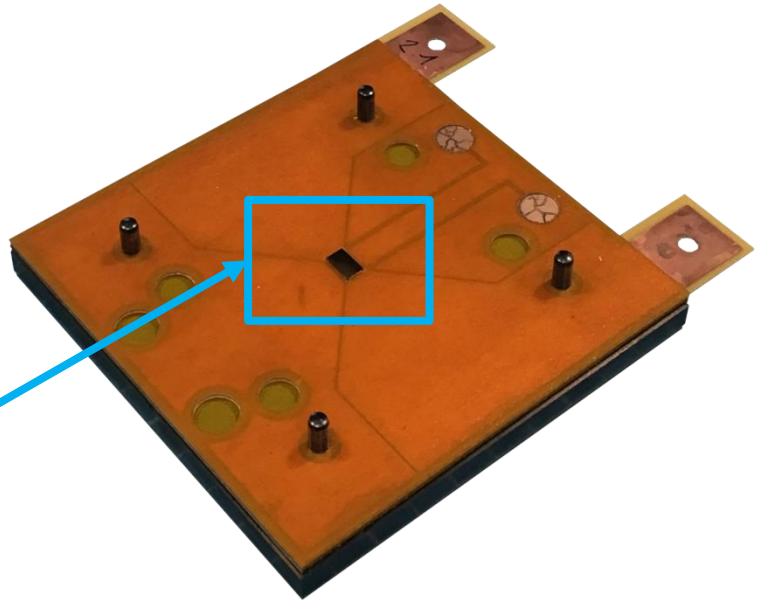


Figure 9: Stacking of the different elements of the prototype

MANUFACTURING PROCESS

Test vehicles assembly

Preparation of the support
Macro-nano structured PCB substrate
Prepreg Arlon 35N 106
Core Arlon 35N
Bare die

- **Prepreg Arlon 35N 106**

a. Laser cut-out.

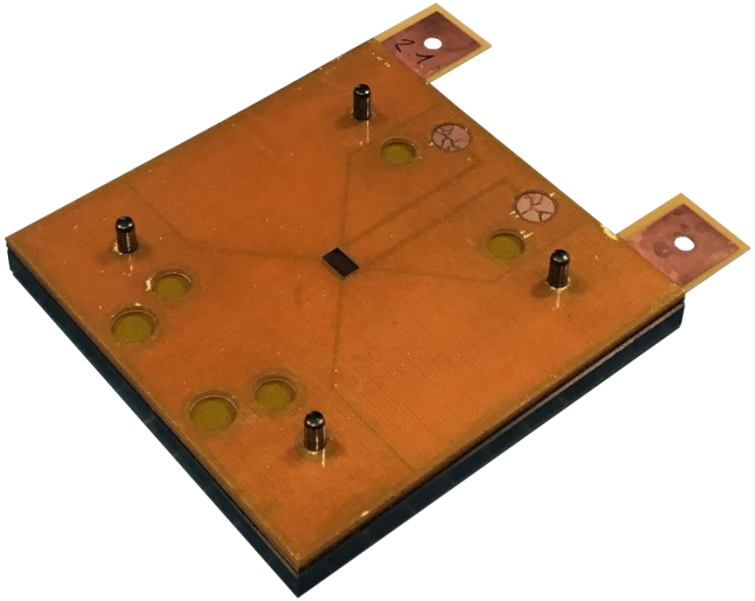


Figure 9: Stacking of the different elements of the prototype

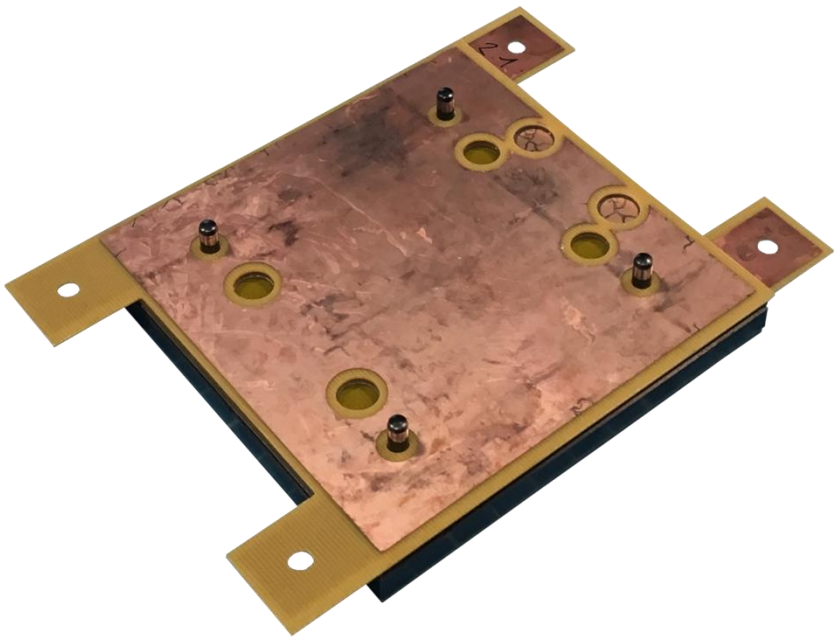
MANUFACTURING PROCESS

Test vehicles assembly

Preparation of the support
Macro-nano structured PCB substrate
Prepreg Arlon 35N 106
Core Arlon 35N
Bare die
Prepreg Arlon 35N 106

- **Macro-nano structured PCB substrate**

a. Deoxidized by 10% sulfuric acid treatment;
b. 12 hours annealing at 120°C.



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MANUFACTURING PROCESS

Test vehicles assembly

Preparation of the support
Macro-nano structured PCB substrate
Prepreg Arlon 35N 106
Core Arlon 35N
Bare die
Prepreg Arlon 35N 106
Macro-nano structured PCB substrate

- **Closing of the support**

a. Implementation of the release films and the press pad and therefore the top plate;
b. 1 hour under vacuum;
c. Protective layers on both sides.

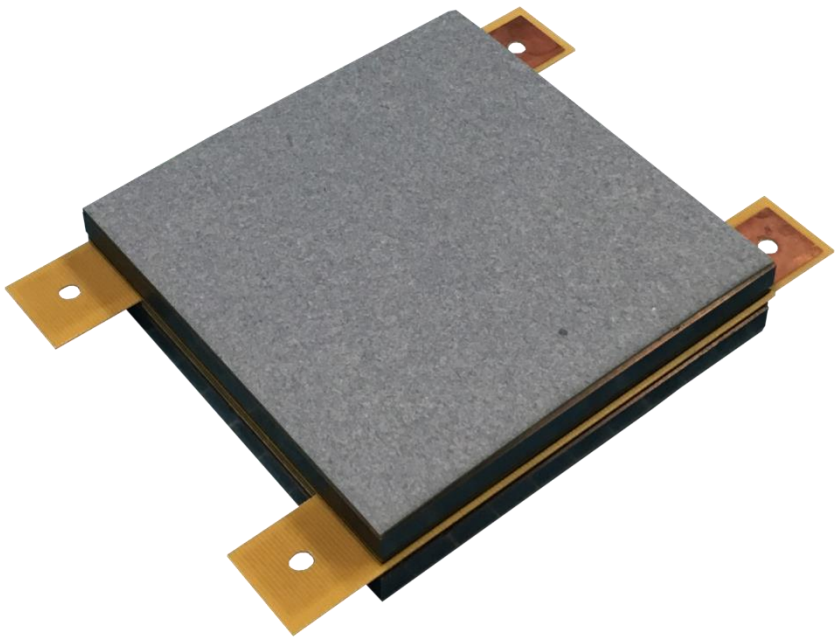

Figure 9: Stacking of the different elements of the prototype

MANUFACTURING PROCESS

Test vehicles assembly

Preparation of the support
Macro-nano structured PCB substrate
Prepreg Arlon 35N 106
Core Arlon 35N
Bare die
Prepreg Arlon 35N 106
Macro-nano structured PCB substrate
Closing of the support

- **Pressing of the prototype**

a. Pressing with Arlon 35N recommended profile;
b. Removing of the assembly from the support.

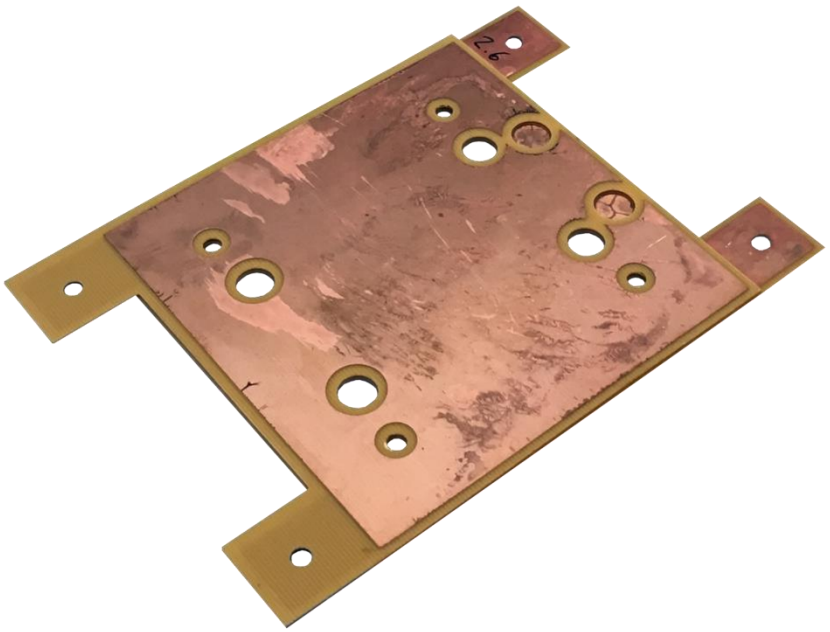

Figure 9: Stacking of the different elements of the prototype

MANUFACTURING PROCESS

Test vehicles assembly

Preparation of the support
Macro-nano structured PCB substrate
Prepreg Arlon 35N 106
Core Arlon 35N
Bare die
Prepreg Arlon 35N 106
Macro-nano structured PCB substrate
Closing of the support
Pressing of the prototype

- **Caption**

a. Measuring pads of (**A**) bottom and (**B**) top substrate;
b. Power connectors of (**C**) top and (**D**) bottom substrate.

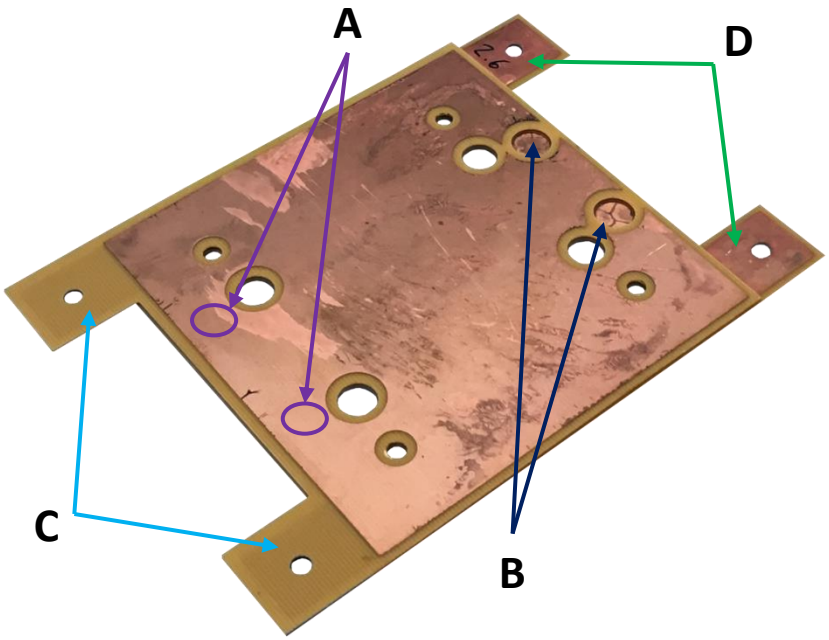

Figure 9: Stacking of the different elements of the prototype

OUTLINE

Introduction

Context

Manufacturing process

Experimental results

Conclusion

EXPERIMENTAL RESULTS

Electrical characterization

Interconnection assembly

- Bare PCB substrate (a)
- Assembled by thermo-compression of a prepreg (b)
- To macro-nano structured (≈ 100 µm) PCB substrate (c)

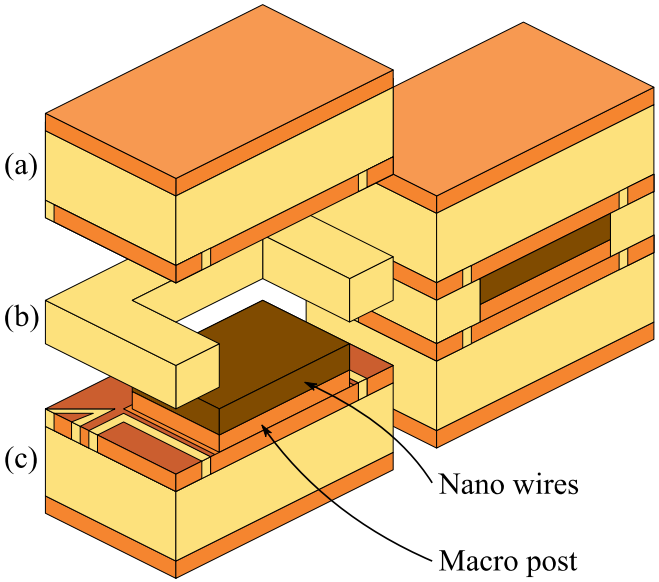

Figure 10: Schematic of the characterization assembly

Characterization

Two assemblies with different prepreg (interlayer)

- A 120 µm layer of prepreg (study case A)
- A 80 µm layer of prepreg (study case B)

EXPERIMENTAL RESULTS

Electrical characterization

Kelvin measurement

- Constricted area electrical resistance (R_{TOP} and R_{BOT})
- Interconnection one (R_{INT})
- Voltage measure by measuring pads (K_{TX} and K_{BX} shunted)
- Current source by power connectors (P_{TX} and P_{BX} shunted)

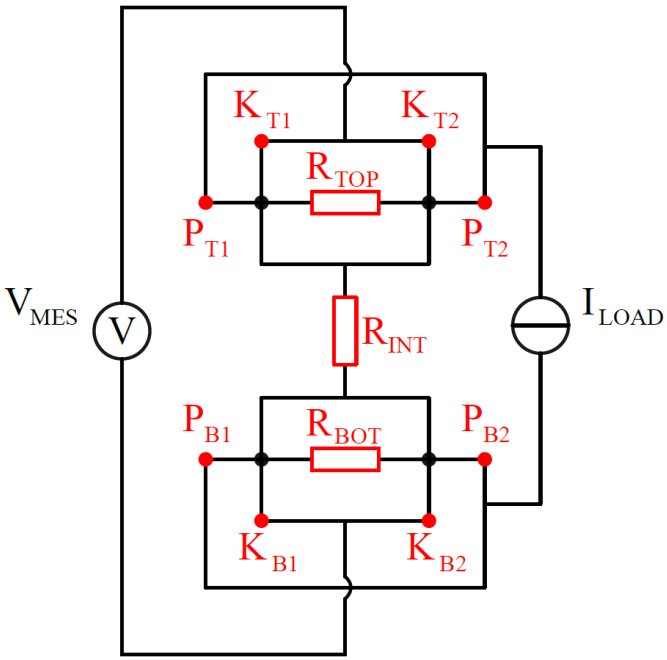

Figure 11: Electrical circuit wiring for interconnection kelvin measurement

Interconnection values

Proto. = 2 x Interco. + Die

Sample (Interlayer)	**Int. A** (120µm)	**Int. B** (80 µm)	**Die**	**Proto.** (490 µm)
Electrical Resistance	10 mΩ	30 µΩ	100 µΩ	160 µΩ

NB: Table's +/- 5% rounded measurements taken at room temperature

EXPERIMENTAL RESULTS

Electro-thermal characterization

Evaluating of thermal resistance (R_{th}) by

1. Controlling power flux on one side (P)
2. Measuring applied heat on the other (ΔT)

Constricted tracks

- ✓ Generating the heat by current applying
- ✓ Measuring of the temperature

Furthermore

- ➢ Simulation of the power dissipated by the interconnection environment
- ➢ Assembly modification to maintain the temperature (accurate ΔT)

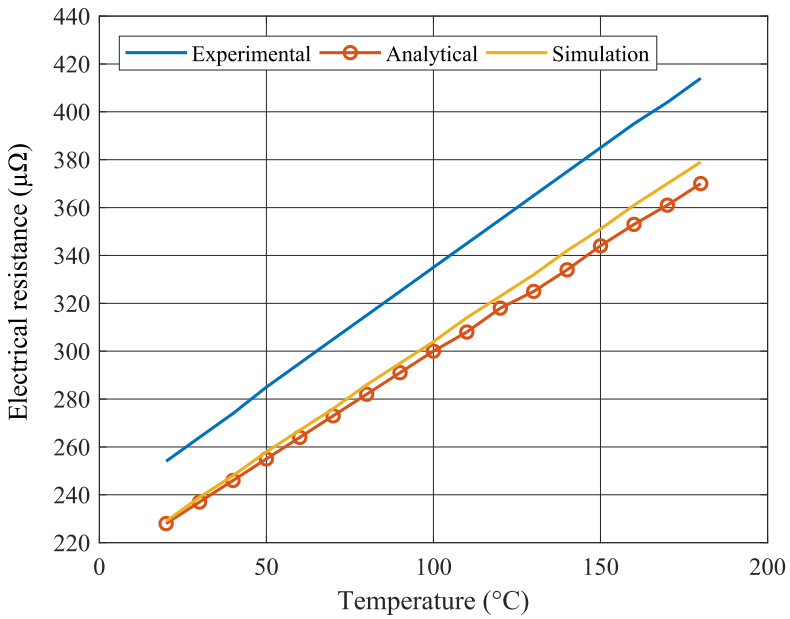

Figure 12: Experimental, analytical and simulated curves of the constriction track

OUTLINE

Introduction

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Manufacturing process

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CONCLUSION

Evolution of the power modules

- Power semiconductor devices integration is sought

Proposed approach

- PCB-embedding technology
- Macro-nano structured interconnections

Best advantages

- Flex interconnection
- Double side heat dissipation
- Low stray inductances
- Manufacturing process (common electronics product line and mass production)

Experimental results

- Parallel electroplating and electro-etching validated
- Low interconnection resistance approximatively 115 $\mu\Omega.cm^{-2}$
- Thermal resistance's measure in progress

Thank you for your attention.

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This work is carried out as part of a partnership between Mitsubishi Electric R&D Centre Europe, Rennes and the Laplace laboratory of the University of Toulouse.

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